AMENDMENTS TO THE SPECIFICATION:

Kindly replace the paragraph beginning at page 14, line 13, with the following amended paragraph:

The external address generator 112 is connected to the bus interface section 104 via an address signal bus 151 and to the external device 113 via an address signal bus [[130]] 131. The external device controller 111 is connected to the bus interface section 104 via a control signal bus 152, and to the external device 113 via a control signal bus [[131]] 132. The external device controller 111 is input the data pre-read instruction signal 120 from the bus master-A 101, and an address signal EADDR from the address signal bus 151.

Kindly replace the paragraph bridging pages 14 and 15 with the following amended paragraph:

A write data input terminal of the data holder 106 is connected to the bus interface section 104 via a write data signal bus 154, and a write data output terminal is connected to a write data input terminal of the data buffer 107. A read and write data input/output terminal of the data buffer 107 is connected to the external device 113 via a data signal bus [[132]] 133, and read data input terminals of the data holder 108 and the pre-read data storage 109 are respectively connected to the read data output terminal thereof.

Kindly amend the paragraph beginning at page 16, line 11, with the following remaining paragraph:

The whole of the address signal bus [[130]] 131 between the external address generator 112 and the external device 113, the control signal bus [[131]] 132 between the external device controller 111 and the external device 113, and the data signal bus [[132]] 133 between the data buffer 107 and the external device 113 is referred to as an external bus. The signals transmitted to the respective buses are specified by using names of an external bus address signal, an external bus control signal, and external bus read data signal.